A case study on the effectiveness of Wafer-Ring Multi-sites test handler to improve of Production Output

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***Abstract*— The conventional method allows testing of only one chip at a time (single-site testing). However, due to advancements in testing procedures, current test technologies are able to conduct dual-sites testing, quad-sites testing, octal-sites testing, 16-sites testing, 32-sites testing, and so on. In line with this, the multi-site testing approach is a method that increases the number of chips that can be tested in a single touch-up. This method allows more chips to be tested per hour, thus improving the testing throughput. In this research the author take the initiative to develop a multi-sites throughput model to investigate the effectiveness of multi-site testing approach on improving the testing throughput. In the case study, five multi-site configurations were applied. These configurations were single-site, quad-sites, octal-sites, ×16-sites, and ×32-sites. A hypothesis was analyzed by using one-way ANOVA and Post Hoc Test.**

***Index Terms*— multi-site, test handler, semiconductor testing, multi-sites testing model.**

I. INTRODUCTION

The continuous decrease in the selling price of electronic devices limits the profit margin of manufacturers, and also leads to the constriction of the selling price of semiconductor chips.

The cost of fabricating semiconductor chips has been reduced over the past 20 years. From 2012 onwards, testing cost has become the deciding factor of profit margin in the manufacture of semiconductor chips. Consequently, reduction in testing cost has become the common goal of semiconductor manufacturers around the world. Failure to reduce testing cost can result in a semiconductor chip manufacturing company losing its competitiveness in the market. An effective way to reduce testing cost is to decrease testing time. Decreasing testing time also increases testing throughput. To achieve this objective, the performance and speed of the test equipment need to be improved. Therefore, the chip-transfer time and chip-testing sequence need to be developed to allow semiconductor chips to be tested rapidly.

To improve the testing process, a number of new technologies have been developed; one of them is the multi-site approach. Multi-site testing is an effective and popular method for increasing throughput and reducing testing cost (Higgins, 2005). In this method, multiple semiconductor chips are tested parallel to a single test-equipment setup (Lew, 2006). This approach provides more benefits than the single-site test approach with regard to test throughput and testing cost reduction (Volkerink, 2002).

However, the advancement of technology leads to an increase in capital equipment investment. The failure of a new technology to provide the expected throughput outcome increases testing costs. Therefore, studying equipment efficiency in relation to capital equipment investment is important to ensure that the semiconductor industry advances in the right direction and to incur lower testing costs while maintaining adequate profit margins.

II. MULTI-SITE THROUGHPUT MODEL DEVELOPMENT

Production output consists of three fundamentals: testing output (throughput), testing yield, and the equipment utilization percentage. Detailed explanations for these fundamentals are as follows.

$$UPH_{good} = \frac{3600 \times N}{((1-MSE)(N-1)(t_i+i_i) + (t_i+i_i))} \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100 \right) \quad (1)$$

Equation 1 was developed to calculate the production throughput whereby the throughput obtained is the tested good product by take into account the testing yield whereby the testing yield mean that the percentage of tested good.

The equation 1 was integrated with the Multi-sites efficiency (MSE) as well so that the comparison between the multi-sites versus the multi-sites efficiency (MSE) can be obtained.

To integrate the MSE into the equation, the throughput equation from Evans (1999) as shown in equation 2 need to further enhance. Following discuss step by step on how the MSE was integrated into the throughput equation.

$$UPH_{insertions} = \frac{3600 \times n}{t_{ms} + i_{ms}} \quad (2)$$

where:

- tms is the multi-site test time, that is, the time spent to complete the testing of a semiconductor chip.
- ims is the multi-site indexing time, that is, the semiconductor chip exchange time within the tested chip replaced with a new untested chip.
- n is the number of test sites, that is, the number of semiconductor chips tested in a single contact.

To achieve the integration with the MSE, the throughput equation developed by Evans (1999), shown as Equation 2, is enhanced by integrating the MSE model developed by Kelly (2008). The MSE proposed by Kelly is presented as Equation 3:

$$MSE = \left[1 - \frac{\Delta t}{\Delta N(t_1)}\right].100\% \quad (3)$$

where:

- Δt is the change in testing time between single-site and multi-site testing; and
- ΔN is the number of different test sites between single-site and multi-site testing.

Equation 3 is further derived, as shown in Equation 4.

$$MSE = \left[1 - \frac{(t_{MS} - t_1)}{(N-1)(t_1)}\right].100\% \quad (4)$$

where:

- t_{MS} is the multi-site test time, and t_1 is the single-site test time; and
- N is the number of test sites for multi-site testing.
-

The test handler affects testing throughput. Therefore, the test handler indexing time has to be included as part of the MSE equation. In doing so, Equation 5 is derived by including the indexing time (i), as follows:

$$MSE = 1 - \left[\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N-1)(t_1+i_1)}\right].100\% \quad (5)$$

For the integration of the equations to work, one must have prior understanding of the relationship between the throughputs and MSE. To determine the relationship between MSE and multi-site, the variables of MSE, which is related to the throughput, need to be understood. Equation 2 and Equation 5 show that the multi-site test time (t_{ms}) and multi-site indexing time (i_{ms}) are common variables in both equations.

In Equation 5, t_{MS} and i_{MS} represent multi-site test time and indexing time. Therefore, to clearly derive the relationship between t_{ms} and i_{ms} in relation to MSE, the integration process shown in Figure 1 is carried out.

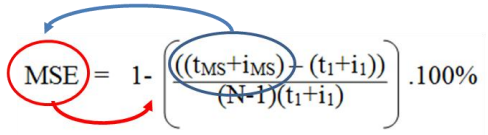

Figure 1 Deriving the Relationship between t_{ms} and i_{ms} with MSE

As Figure 1 illustrates, t_{ms} and i_{ms} move to the left side of the equation, whereas MSE moves to the right side. The final computation for the equation of t_{ms} and i_{ms} in relation to MSE is derived and shown in Equation 6.

$$(t_{MS} + i_{MS}) = (1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1). \quad (6)$$

Finally, Equation 6 is integrated into Equation 2 to obtain the computation for testing throughput, which includes MSE as part of the calculation. Figure 2 below shows the computation of the integration, and the complete integration is illustrated in Equation 7:

$$UPH_{insertions} = \frac{3600 \times n}{t_{ms} + i_{ms}}$$

$$(1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1)$$

Figure 2 The Computation of the Integration of Equation 6 into Equation 2

$$UPH_{insertions} = \frac{3600 \text{ X } N}{((1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1)),} \quad (7)$$

where:

$UPH_{insertions}$ are represented by the testing output in one hour.

III. Wafer-Ring Test-Equipment

The concept of the wafer-ring testing handling is similar to that of the lead frame strip testing. However, this handling method attaches the lead frame on top of the wafer ring. A photograph of the wafer-ring is shown in Figure 3. This testing method is used on lead-less packagers such as wafer-level packaging, ball-guided assembly, chip scale packaging, and so on.

Similar to lead frame strip-testing handling, the semiconductor chip is tested without singulating the chip from the leadframe. As shown in Figure 4 below, the process flow is basically similar to that of leadframe strip- testing handling, the only difference being the wafer ring, which is attached to the two leadframes, is transferred to the Test Area by pick-arm 1 and attached to the test chuck. The test chuck then transfers the wafer ring to the Test Area and, similar to the lead-frame testing handling, the wafer is punched to connect to the test socket/contactor. The test chuck moves in X and Y directions to test the entire chip on the wafer ring. The completely tested wafer ring is transferred to the output area by pick-arm 2. A photograph of the wafer ring test chuck is shown in Figure 5 below.

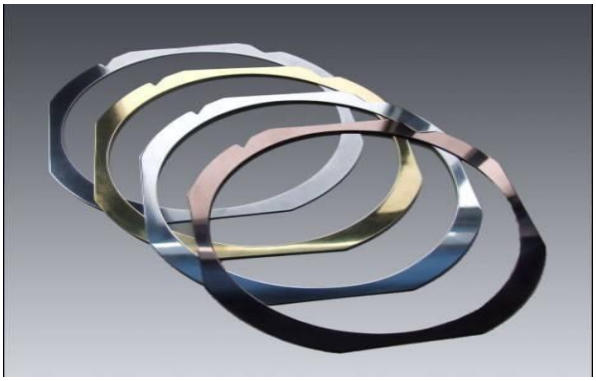

Figure 3 Example of Wafer Rings

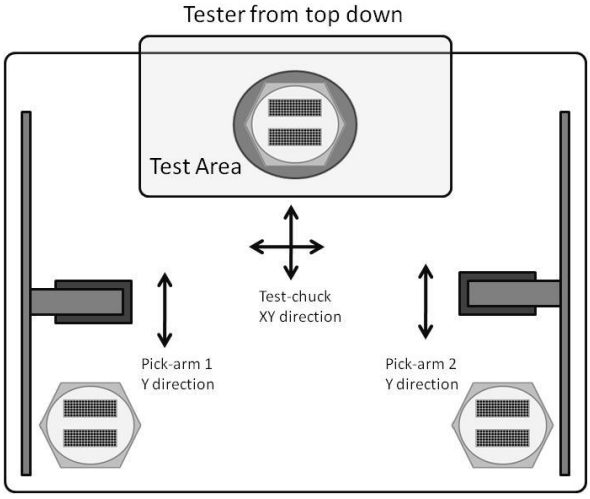

Figure 4 The Process Flow of the Wafer-Ring Testing-Handling Test Equipment

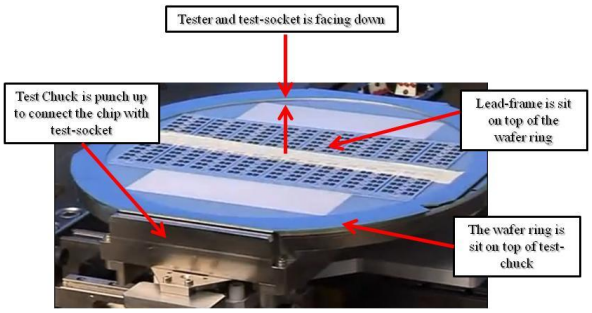

Figure 5 The Test Chuck of the Wafer-Ring Testing Handling

The test site configuration setup for the case study is explained in the subsequent section.

The wafer-ring test equipment can support the configuration of X32-sites. Wafer-ring testing attaches two lead frames on a wafer ring. Test site configurations are on the lead-frame layout for the setting from a single-site to X32-sites.The top-view illustration of the lead frame is shown in Figure 6 below:-

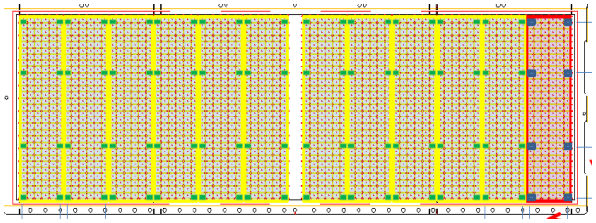

Figure 6 Top View Illustration of the Lead Frame

For single-site testing, the wafer-ring test equipment is configured to allowcontact with one chip (represented by a bluebox) on the leadframe per touchdown, and is indexed to the next chip in the direction of the red arrow,as shown in Figure 7 below. The test equipment completes testing the entire chip in the first row before moving on to the second row to perform the same sequence.

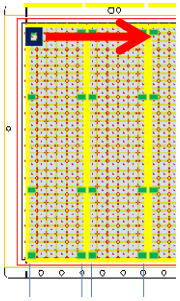

Figure 7 Single-site Testing Sequence for Wafer Ring Testing

The sequence for quad-site testing is similar to that for single-site testing. However, the test equipment comes in contact with four chips per touchdown, as shown in Figure 8 below. After testing the first four chips, the equipment will then index toward the direction of the red arrow. After testing the first row, the equipment will continue testing the second row by following the same sequence.

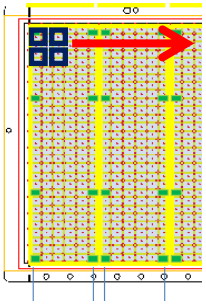

Figure 8 Quad-sites Testing Sequence for Wafer Ring Testing

Octal-site, X16-site, and X32-site testing have a sequence similar to that of single-site and quad-site testing. However, for octal-site testing, the test equipment comes in contact with eight chips per touchdown, followed by 16 chips per touchdown for X16-site testing, and 32 chips per touchdown for X32-site testing, as shown in Figures 9, 10, and 11, respectively.

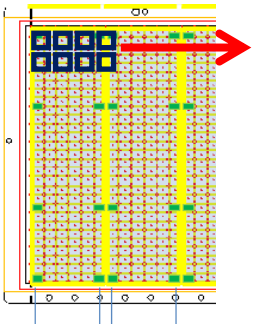

Figure 9 Octal-sites Testing sequence for Wafer-Ring Testing

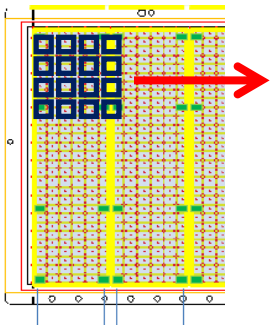

Figure 10 X16-sites Testing Sequence for Wafer-Ring Testing

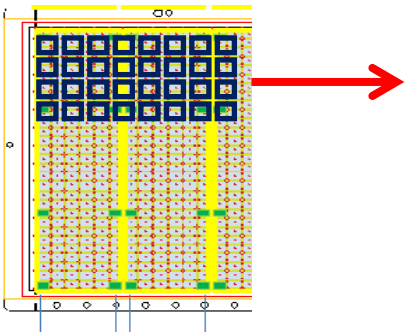

Figure 11 X32-sites Testing Sequence for Wafer-Ring Testing

After defining the test-site configuration for both types of test equipment, the next step is to decide the indexing time and test-time data collection area for the test equipment.

IV. ANALYSIS RESULT

This study only considers the pure indexing time and rejects any indexing time that causes a slow down because of external factors such as wafer-ring transferring process, loading-and-unloading process, equipment jamming, and so on. Production data are only accepted if no external factors such as handler downtime, tester downtime, and others are found.

This study only focuses on the area marked by the red circle in Figure 12 below:-

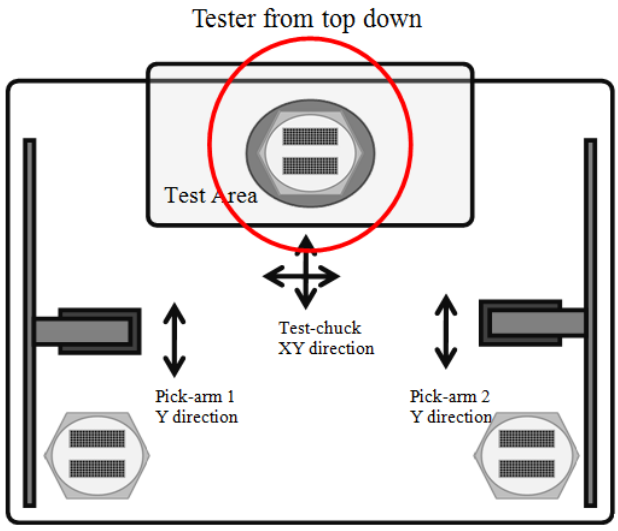

Figure 12 Focus of the Research Area

The indexing time is considered valid when the wafer-ring is within the red circle. Once the wafer-ring gets outside the red circle for the wafer-ring exchange, the delay time for the exchange is no longer considered because it is an external factor. Otherwise, if the wafer-ring test equipment stops because of any external factors such as jamming, equipment downtime, time of handler and tester, new production lot loading, unloading time, and others, then the indexing time is not considered valid.

The test-time is considered valid if no external factors, such as tester downtime and chip contacting problems, cause a high rejection rate of the chip being tested.

To collect sufficient data for the cost-of-test, data size of the 30 sets of production lots for each test site configuration (single-site, quad-sites, octal-sites, X16-sites, and X32-sites) has to be collected (the data type to be collected is discussed in the following section). Each set of data contains 100 trial runs of the test-equipment setup, and thus, the 30 sets of data contain 3,000 test equipment trial runs. Five test-site configurations are employed in the case study; therefore, 30 sets are used for each test-site setup. The five types of test-site configurations contain 150 sets of data, including 15,000 trial runs on test equipment for

As shown in ***Equation 1,*** production output involves two parts. The first part is the testing throughput ($UPH_{insertion}$) and the second is the testing yield or good-unit yield.

Testing Throughput ($UPH_{insertion}$)

For the testing throughput, MSE must be obtained. MSE is calculated using ***Equation 5*** as follows:-

$$MSE = 1 - \left[\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N-1)(t_1+i_1)} \right] .100\% \quad (5)$$

The example of the calculation for single-site testing configuration is as follows:-

$$MSE = 1 - \frac{\left[\left(0.73 + \right) - \left(0.73 + \right)\right]}{\left[1\right]\left[0.73 + \right]} X100\%$$

MSE = 100%.

The summary of MSE results is shown in Table 1 below:-

Table 1 MSE for Wafer-Ring Test equipment

Multi-site efficiency

Number of Sites	Multi-sites Efficiency	Compared with Single-	Compared with Quad-	Compared with Octal-	Compared with X16-
Single-site	100.00%	0.00%			
Quad-sites	36.34%	-63.66%			
Octal-sites	32.49%	-67.51%	-10.59%		
X16-sites	30.88%	-69.12%	-15.02%	-4.96%	
X32-sites	24.11%	-75.89%	-33.67%	-25.81%	-21.94%

MSE for wafer-ring quad-site testing is 36.34%, which is a 63.66% reduction of that for single-site testing. MSE for octal-site testing is reduced by 67.51% but is higher than that of quad-site testing by 10.59%. MSE of the X16-site testing is only 30.88% compared with that for single-site testing, thus displaying an approximately 69.12% decrease. The worse MSE for wafer-ring test equipment is exhibited by the X32-site testing, with only 24.11%. After obtaining MSE, testing the throughput is calculated. Variables that affect testing the throughput are the indexing time and test time. A summary of the indexing time and test time for wafer-ring test equipment is provided in Table 2 below:-

Table 2 Indexing Time and Test Time-Data for Wafer-Ring Test-equipment

0.7 Second Test-time per		Slow down percentage			
Test-sites configuration	Average Index Time	Compared with Single-	Compared with Quad-	Compared with Octal-	Compared with X16-site
Single-site	0.34	0.00%			
Quad-sites	0.34	-0.34%			
Octal-sites	0.35	0.73%	1.07%		
X16-sites	0.352	2.18%	2.52%	1.44%	
X32-sites	0.354	2.76%	3.11%	2.02%	0.57%
		Slow down percentage			
	Average Test Time	Compared with Single-site	Compared with Quad-site	Compared with Octal-site	Compared with X16-site
Single-site	0.73	0.00%			
Quad-sites	2.77	281.85%			
Octal-sites	5.78	696.65%	108.63%		
X16-sites	11.81	1528.17%	326.39%	104.38%	
X32-sites	25.89	3468.84%	834.63%	347.98%	119.19%
		Slow down percentage			
	Total	Compared with Single-site	Compared with Quad-site	Compared with Octal-site	Compared with X16-site
Single-site	1.07	0.00%			
Quad-sites	3.11	190.98%			
Octal-sites	6.13	472.55%	96.77%		
X16-sites	12.16	1036.78%	290.67%	98.55%	
X32-sites	26.24	2352.72%	742.92%	328.38%	115.76%

The indexing time for the wafer-ring test equipment is almost constant, between 0.34 second and 0.35 second for all test-site configurations. However, test time increases as the number of test sites increases. Single-site testing only requires 0.73 seconds, whereas quad-site configuration increases by about 281.85% relative to single-site, which only requires 2.77 seconds to complete the testing. Octal-site testing requires 5.78 seconds, which is 696.65% slower compared with single-site testing, and 108.63% slower compared with quad-site testing. Test time for the X16-site further increases to 11.81 seconds, whereas the X32-site configuration requires 25.89 seconds to complete testing or 3468.84% slower compared with single-site testing. Total time slows down because of the test time but the indexing time remains constant.

The summary for the wafer-ring test-equipment testing throughput results is provided in Table 3 below:-

Table 3 Testing Throughput for Wafer-Ring Test-Equipment

Throughput

Number of Sites	Throughput	Compared with Single-site	Compared with Quad-site	Compared with Octal-site	Compared with X16-site
Single-site	3365	0.00%			
Quad-sites	4626	37.47%			
Octal-sites	4702	39.73%	1.64%		
X16-sites	4736	40.75%	2.39%	0.73%	
X32-sites	4390	30.47%	-5.09%	-6.63%	-7.30%

Single-site configuration produces 3,365 chips in one hour, whereas quad-site configuration produces approximately 37.47% more chips or 4,626 chips per hour. Furthermore, octal-site configuration is more efficient than quad-site configuration by 1.64%, producing 4,702 chips per hour. The X16-site configuration is capable of producing 4,726 chips per hour, or 0.73% and 2.39% better than octal-site and quad-site configurations, respectively. Moreover, the X16-site configuration achieves a 40.75% improvement over that of single-site configuration. However, the X32-site configuration tests slower by approximately7.30% compared with the X16-site configuration, producing only 4,390 chips per hour. This result is still better by 30.47% compared with single-site configuration.

Testing Yield Percentage

Testing yield is one of the factors affecting the cost-of-test. Testing yield percentage data collected from the wafer-ring test-equipment setup is shown in Table 4 below:-

Table 4 Testing Yield Percentage for Wafer-ring Test equipment

Test site	Single-site	Quad-sites	Octal-sites	X16-sites	X32-sites
Yield % Average	99.70%	99.70%	99.68%	99.58%	99.61%
Difference %					
Compared with Single-site	0.00%	0.00%	-0.02%	-0.12%	-0.09%
Compared with Quad-sites	0.00%	0.00%	-0.02%	-0.12%	-0.09%
Compared with Octal-sites	0.02%	0.02%	0.00%	-0.10%	-0.07%
Compared with X16-sites	0.12%	0.12%	0.10%	0.00%	0.03%
Compared with X32-sites	0.09%	0.09%	0.07%	-0.03%	0.00%

Figure 13 shows that the single-site configuration achieves a testing yield of 99.70%, whereas the quad-site configuration achieves 99.70%, which remains constant. The octal-site configuration produces a 99.68% testing yield, which is a reduction of 0.02% compared with the single-site and quad-site configurations.

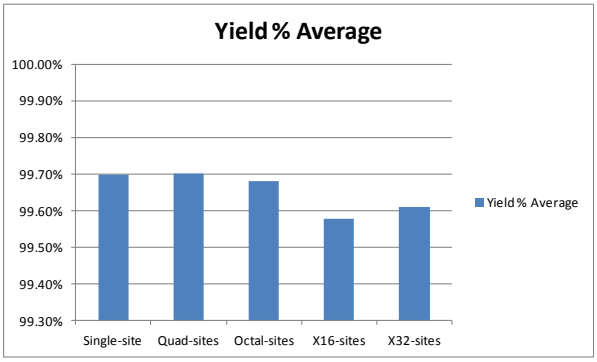

Figure 13: Testing Yield Percentage Graph for Wafer-ring Test equipment.

Testing yield for the X16-sites is 99.58%, which is the lowest among the test site configurations, followed by the X32-site testing at 99.61%. The data show that testing yields for all test-site configurations are relatively uniform and they do not affect increments of test sites.

Production Output

After obtained of the testing throughput and the testing yield, then the production output was calculated with equation 1 as shown below:

$$UPH_{good} = \frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1)+(t_1+i_1))} \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100 \right) \quad (1)$$

The summary of the production output for the entire test-sites are tabulated in table 5:

Table 5 Testing Production Output

Number of Site	Testing Throughput	Testing Yield	Production Output
Single-site	3365	99.70%	3355
Quad-sites	4626	99.70%	4612
Octal-sites	4702	99.68%	4687
X16-sites	4736	99.58%	4716
X32-sites	4390	99.61%	4373

After obtained the production output as shown in table 5, following section discuss the hypothesis analysis.

Hypothesis Analysis

An alpha level of 0.05 is used for the analysis. As previously discussed, five independent levels of configurations (a) are selected, namely, single-site, quad-sites, octal-sites, X16-sites, and X32-sites. Each independent level contains 30 data sets (n). In this case, the following data are determined:-

a = 5 independent levels,
n = 30 sets of data,
N = 150.

Therefore, the degrees of freedom are calculated as

dfBetween= 5 -1 = 4,
dfWithin = 150 – 5 = 145,
dfTotal= 150 – 1 = 149.

From the degrees of freedom between and within, which is (4,145), refer to the F-Table, with the critical value obtained as 2.3719. As indicated in the previous chapter, if the F-value is smaller than the critical value, then the null hypothesis is accepted; otherwise, the null hypothesis is rejected.

a. Hypothesis 1: Multi-site versus MSE

Analysis of Hypothesis

The hypothesis conditions that need to be tested are listed below.

H_0: Improving the number of test sites has no effect on MSE.
H_1: Improving the number of test sites has an effect on MSE.

The MSE data are rated as dependent levels on a scale of 1 to 10, as shown in Table 6 below:-

Table 6 Scale of MSE Dependence Level

MSE	Scale
100.00%	10
92.31%	
92.30%	9
84.61%	
84.60%	8
76.92%	
76.91%	7
69.22%	
69.21%	6
61.53%	
61.52%	5
53.83%	
53.82%	4
46.14%	
46.13%	3
38.44%	
38.43%	2
30.75%	
30.74%	1
23.05%	

The dependence level of the wafer-ring test equipment MSE are rated from 1 to 10, with 1 representing the worst MSE performance and 10 representing the best MSE performance.

Table 7 ANOVA results for MSE

ANOVA Table

	SS	df	MS	F
Between	1734.24	4.00	433.56	4448.08
Within	14.13	145.00	0.10	
Total	1748.37	149.00	11.73	

Table 7 above shows that the F-value for the wafer-ring test-equipment MSE is 4448.08, which is greater than the critical value of 2.3719. Thus, the null hypothesis for the wafer-ring test-equipment MSE is rejected. This finding

shows that improvement of the test sites does have an effect on the wafer-ring MSE. This research further analyzes the data through post hoc test to determine the effect of one test site to another.

The summary for the MSE post hoc test is presented in Table 8 below:-

Table 8 Analysis Results of the *Post Hoc* Test

***Post Hoc* Test**

Independence Level	F-value	Analysis Result
Single vs. Quad	4981.13	Different - Reject the null hypothesis
Single vs. Octal	5123.78	Different - Reject the null hypothesis
Single vs. X16	6390.85	Different - Reject the null hypothesis
Single vs. x32	8156.25	Different - Reject the null hypothesis
Quad vs. Octal	1.01	No Difference - Accept the null hypothesis
Quad vs. X16	87.72	Different - Reject the null hypothesis
Quad vs. X32	389.46	Different - Reject the null hypothesis
Octal vs. X16	69.93	Different - Reject the null hypothesis
Octal vs. X32	350.86	Different - Reject the null hypothesis
X16 vs. X32	107.52	Different - Reject the null hypothesis

Referring to Table 8 above, the highest post hoc test F-value shows that the significant difference is greater. For the MSE dependence factor level, a higher F-value means that the MSE is worse when compared with the single-site testing. The X32-sites have the worse MSE performance, followed by the X16-sites, octal-sites, and quad-sites. The quad-site and the octal-site testing do not show significant changes for the MSE, and the null hypothesis is thus accepted for this analysis. Other test-site comparisons show that test-site improvements have an effect on MSE.

This analysis shows that the MSE decreases when the number of test sites is increased.

b. Hypothesis 2: Multi-sites versus Throughput Improvement

An analysis of hypothesis 2 is provided in the following paragraphs.

Analysis of Hypothesis

The hypothesis for the throughput analysis is designed as follows.

H_0: Improvement of test site has no effect on throughput.
H_1: Improvement of test site has an effect on throughput.

The dependence level for testing throughput is rated using a scale of 1 to 10, as shown in Table 9 below:-

Table 9 Scale of Testing Throughput Dependence Level

Testing Throughput	Scale
5093	10
4902	
4901	9
4710	
4709	8
4519	
4518	7
4327	
4326	6
4135	
4134	5
3944	
3943	4
3752	
3751	3
3560	
3559	2
3369	
3368	1
3186	

Table 10 ANOVA results for Testing Throughput

ANOVA Table

	SS	df	MS	F
Between	1086.49	4.00	271.62	630.17
Within	62.50	145.00	0.43	
Total	1148.99	149.00	7.71	

The one-way ANOVA results for the wafer-ring testing throughput are shown in Table 10 above. The F-value is 630.17, which is higher than the critical value of 2.3719. In this case, the null hypothesis is rejected and analysis results show that improving the test site has an effect on testing throughput. Data are further analyzed using post hoc test for test site to test site comparison. The results of the post hoc test are shown in Table 11.

Table 11 *Post Hoc* Test analysis Results for Testing Throughput

Post Hoc Test

Independence Level	F-value	Analysis Result
Single vs. Quad	382.81	Different - Reject the null hypothesis
Single vs. Octal	422.25	Different - Reject the null hypothesis
Single vs. X16	446.84	Different - Reject the null hypothesis
Single vs. x32	272.83	Different - Reject the null hypothesis
Quad vs. Octal	0.97	No Difference - Accept the null hypothesis
Quad vs. X16	2.47	Different - Reject the null hypothesis
Quad vs. X32	9.29	Different - Reject the null hypothesis
Octal vs. X16	0.35	No Difference - Accept the null hypothesis
Octal vs. X32	16.25	Different - Reject the null hypothesis
X16 vs. X32	21.35	Different - Reject the null hypothesis

The results of the post hoc test for the wafer-ring test equipment show that no significant difference in throughput improvement is found compared with the quad-site and octal-site testing, or between the octal-site and the X16-site testing. Others test-site configuration comparisons show a significant difference and do have an effect on throughput improvement. Referring to Table 5.42, the post hoc test analysis results show that the X16-site configuration has a higher significant difference relative to the single-site configuration. Thus, the X16-sites produce higher throughput improvement. The octal-sites produce the second highest throughput improvement, followed by the quad-site testing. The X32-site testing for the wafer-ring test equipment is still the lowest. This finding is similar to the results obtained for the pick-and-place test-equipment setup.

V. CONCLUSION

The validation through the case study shows that total cost and production output affect the cost of testing. Production output is affected by MSE, and a higher MSE results in better production output.

The MSE is determined by the indexing time, test time, and number of test sites. Production output increases when the indexing time and test time is decreased, and the increment in the number of test sites also contributes to the improvement of the production output. However, if the increment in the number of test sites affects the indexing time and test time is increased at the same time, then the MSE decreases. A lower MSE results in lower production output. Therefore, a combination of the three variables, namely, indexing time, test time, and number of test sites determine the MSE, which contributes directly to production output.

The case study shows that increasing the number of test sites does not guarantee an improvement to throughput and cost of testing. The main reasons for such this scenario are presented in Figures 14 below:-

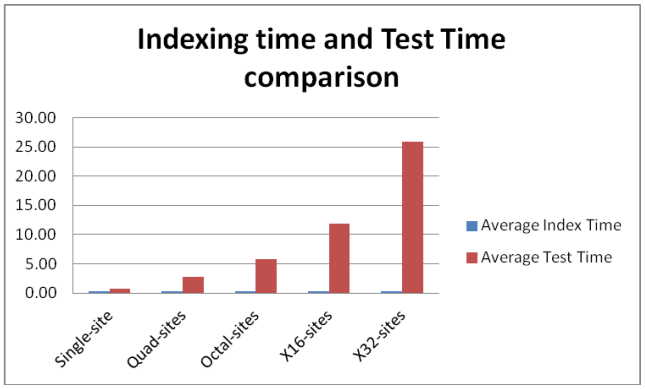

Figure 14 Comparison of the Indexing Time and Test Time for the Wafer-Ring Test equipment.

Testing throughput is the main contributor to the cost of testing. Testing throughput is affected by the indexing time and test time. Figures 14 above show that although the indexing time for the test-equipment setup steadily increases but the test time for the test equipment increases significantly once it reaches higher test-site configuration. Therefore, the test time is the root cause of the decrease in testing speed and the reduction in testing throughput, which result in an increase in testing cost, and consequently, a decrease in profit margin.

Thus, this study concludes that simply increasing the number of test sites is not sufficient to improving testing throughput. Instead, the test time should also be reduced. The test time can be reduced in a number of ways, such as reduced pin-count testing and concurrent test among others.

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