

MANAGING TECHNOLOGY: A CASE STUDY ON THE COST
REDUCTION OF THE MOLDING ASSEMBLY PROCESS
IN THE SEMICONDUCTOR INDUSTRY

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ASIA e UNIVERSITY
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**MANAGING TECHNOLOGY: A CASE STUDY ON THE COST
REDUCTION OF THE MOLDING ASSEMBLY PROCESS
IN THE SEMICONDUCTOR INDUSTRY**

KALIYAPPAN A/L P. RENGANATHAN

**A Thesis Submitted to the School of Graduate Studies of
Asia e University in Fulfillment of the
Requirement for the Degree of
Master of Science (Management)
By Research**

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ABSTRACT

The aim of this study is to investigate the ways in which the semiconductor industry can provide high-quality integrated circuit (IC) assembly services to satisfy customer needs and help companies introduce new products to the market in the shortest time possible. In this study, prototype ICs are assembled in production volumes that not only meet design requirements but also provide quality samples to customers. To increase the cost effectiveness of the component assembly process, the cost of the existing process was determined and a mathematical formula developed to predict the outcome of changes applied in the process (Ragona, 2002).

Over the years, the performance of the semiconductor chip has been significantly improved to meet the current market demand for electronics devices, such as smartphones, personal computers, and car navigation systems. The transistor is the main component of the semiconductor chip. Therefore, the performance of the transistor is important because it significantly influences the density of the transistor per chip (Gordon, 1965).

An increase in the capacity of the transistor per chip increases the manufacturing cost. For this case, various methods and strategies have been implemented to ensure that chip suppliers remain competitive in the market.

This research used the high density substrate approach to analyze the cost of assembly and molding profit through the models which were developed from economics theory of the firm models namely the average cost model and the profit model by integrated in the molding technology aspect particularly the high density substrate. The new models which were developed by the author are the Molding Assembly Cost Model (MACM) and the Molding Assembly Profit Model (MAP).

4 hypotheses were developed to compare the high density substrate versus the low density substrate. The hypotheses for this comparison are the throughput, the yield, the assembly cost and finally the profit.

The author concluded that the high-density substrate approach is sufficient to guarantee of the assembly cost reduction hence improvement of the profit with the condition that the assembly yield must remain stable.

APPROVAL PAGE

I certify that I supervised/read this study. In my opinion, this study conforms to the acceptable standards of scholarly presentation and is fully adequate, in quality and in scope, as a thesis for the fulfillment of the requirements for the degree of Master of Science (Management) by Research.


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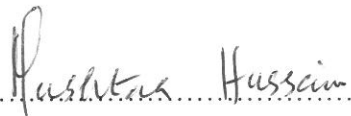
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Declaration

I hereby declare that this thesis is my own work and that all contributions from other persons or sources have been properly and duly cited. I further declare that the materials in this thesis have not been submitted, either in whole or in part, to any other degree in this or any other university. I understand and acknowledge that any breaches in this declaration will constitute academic misconduct, which may lead to my expulsion from the program and/or exclusion from the degree.

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In humility, I thank GOD for the completion of this thesis. The research work presented here was conducted in fulfilment of the requirements of Asia e University for the Master of Science (MANAGEMENT) By Research degree in the School of Management, from September 2010 to September 2014.

I dedicate this work to my beloved parents -the late Mr. P. Renganathan and Mrs. M. Anjalai – whose unfailing support provided the moral encouragement and motivation throughout the course of my research. I record my heartfelt gratitude and dedicate this thesis in memory of my father who passed away on 13 May, 2014.

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TABLE OF CONTENTS

	PAGE
TITLE	I
ABSTRACT	II
SIGNATURE APPROVAL PAGE	IV
DECLARATION PAGE	V
COPYRIGHT PAGE	VI
ACKNOWLEDGEMENT	VII
TABLE OF CONTENTS	VIII
LIST OF TABLES	XIV
LIST OF FIGURES	XV
LIST OF EQUATION	XVII
LIST OF ABBREVIATIONS	XIX
LIST OF APPENDIXS	XXIV

CHAPTER 1

INTRODUCTION

1.0.	OVERVIEW	1
1.1.	Research background	1
1.1.1.	Overview of the Semiconductor chip	1
1.1.2.	Semiconductor manufacturing process	2
1.1.3.	Magnitude of the problem	14
1.1.4.	Manufacturing cost	15
1.2.	Research scope	19
1.3.	Research objective	20
1.4.	Problem statement	21
1.5.	Justification	22
1.6.	Thesis outline	23

CHAPTER 2

LITERATURE REVIEW

2.0.	Overview	24
2.1.	Review of the cost of assembly deduction approach	24
2.2.	The Cost of assembly modelling review	31

CHAPTER 3

RESEARCH METHODOLOGY

3.0.	Overview	48
3.1.	Operational Definitions	48
3.2.	Model development	50
3.3.	Research Methodology	53
3.4.	Research Hypothesis	56

CHAPTER 4

DEVELOPMENT OF ASSEMBLY COST MODEL AND MOLDING PROFIT MODEL

4.0.	Overview	62
4.1.	Development of new assembly cost model	62
4.2.	Identifying the available and model for MACM development	64
4.2.1.	Total Cost	64
4.2.2.	Output	66
4.3.	Variable and MACM integration	68

4.4.	Mold assembly profit model	69
4.5.	Summary	70

CHAPTER 5

MODEL VALIDATION

5.0.	Overview	71
5.1.1.	Molding selection criteria and selection molding equipment	71
5.1.2.	Data collection method	73
5.2.	Research model validation	77
5.2.1.	Calculation of assembly cost	78
5.2.2.	Molding profit model validation	79
5.3.	Analysis of Hypothesis	80
5.3.1.	Analysis of Hypothesis, Different substrate versus throughput improvement	80
5.3.2.	Analysis of hypothesis –different substrate versus Assembly cost reduction	85
5.3.3.	Analysis of hypothesis-different substrate versus Assembly yield	90

5.3.4.	Analysis of hypothesis-different substrate versus profit	93
5.4.	Validation summary	96

CHAPTER 6

Discussion of the model, analysis and research results.

6.0.	Overview	97
6.1.	Remarkable aspect of the research model	97
6.1.1.	Contribution to theory of the firm	98
6.2.	Analysis results and lesson learned from the model validation	99
6.2.1.	Different substrate versus throughput improvement	99
6.2.2.	Different substrate versus cost of assembly	100
6.2.3.	Different substrate versus yield	100
6.2.4.	Different substrate versus profit	101
6.2.5.	Lesson learn from the model and case study	101
6.3.	Summary	102

CHAPTER 7

Conclusion and recommendation

7.0. Overview	103
7.1. Concluding remarks	103
7.2. Case study remarks	104
7.3. Research summary	105
7.4. Recommendation of future research work	106

REFERENCES

108

LIST OF TABLES

	Page
Table 5.1. Variable for the (MACM) molding assembly cost model	77
Table 5.2. Molding processing variables	78
Table 5.3. Summary of the assembly cost	78
Table 5.4. Molding profit	79
Table 5.5. The summary of the throughput of substrate type	81
Table 5.6. Scale of throughput	82
Table 5.7. Throughput one way ANOVA	83
Table 5.8. Post Hoc Test	84
Table 5.9. Cost of assembly	87
Table 5.10. Scale of different substrate type of assembly cost	88
Table 5.11. One way anova result of substrate type	89
Table 5.12. Post host test for different substrate type	89
Table 5.13. Average yield result on different type substrate	90
Table 5.14. Anova result on different type substrate	91
Table 5.15. Post hoc test result on different type substrate	91
Table 5.16. Scale of profit	94
Table 5.17. Anova table on profit	94
Table 5.18. Post hoc test result on Low den vs High den	95
Table 5.19. Comparison between density, yield percentage and profit	95

LIST OF FIGURES

	Page
Figure 1.0. Wafer process flow	3
Figure 1.1. Semiconductor Manufacturing (Potoradi, 2002)	4
Figure 1.2. Semiconductor Process Flow	8
Figure 1.3. Die Attach	9
Figure 1.4. Wire bond	10
Figure 1.5. Transfer Molding	11
Figure 1.6. Ball Mount	11
Figure 1.7. Reflow	12
Figure 1.8. Laser Making	12
Figure 1.9. Singulation	13
Figure 1.10. Tester	13
Figure 1.11. Final Packaging	14
Figure 1.12. Cost per function versus number of functions	16
Figure 1.13. IC Unit shipment and pricing trend	17
Figure 2.1. Test and fabrication cost per transistor (derived from the 1997 National Technology Roadmap for Semiconductor)	28
Figure 2.2. Methods of semiconductor cost of manufacturing improvement graph (Goodall, 2002)	29
Figure 3.1. Conceptual framework	53
Figure 3.2. Cost of assembly modelling	55

Figure 4.1.	Molding Assembly Cost Model (MACM)	63
Figure 4.2.	The integration of variable to the average cost model	68
Figure 5.1.	The Molding Equipment (Top View)	72
Figure 5.2.	Molding Press Photos	73
Figure 5.3.	Low density substrate	73
Figure 5.4.	High density 1 substrate	74
Figure 5.5.	High density 2 substrate	74
Figure 5.6.	High density 3 substrate	74
Figure 5.7.	High density 4 substrate	74
Figure 5.8.	Research data collection area	75
Figure 5.9.	Sample size design	76
Figure 5.10.	Substrate versus yield percentage	92
Figure 5.11.	ASP based on major categories of semiconductors (Turley, 2009)	93

LIST OF EQUATION

		Page
Equation 2.1.	Cost of ownership	32
Equation 2.2.	Total cost	33
Equation 2.3.	Yield cost	35
Equation 2.4.	Total number of parts produced over the life	35
Equation 2.5.	Utilization	36
Equation 2.6.	Formula of cost of ownership	37
Equation 2.7.	Test cost	39
Equation 2.8.	Test cell cost	39
Equation 2.9.	Capital equipment cost	40
Equation 2.10.	Formula of capital equipment cost	40
Equation 2.11.	Test operation cost	41
Equation 2.12.	Total time test cell	41
Equation 2.13.	Production lot change overtime	42
Equation 2.14.	Cost of probe cards	43
Equation 2.15.	Cost of packaging bad parts	43
Equation 2.16.	Test cost model	43
Equation 2.17.	Machine utilization percentage	44
Equation 2.18.	Tester accessory depreciation cost	44
Equation 2.19.	Cost configuration	44
Equation 2.20.	Handling equipment	45

Equation 2.21.	Profit	45
Equation 2.22.	Total cost formula	45
Equation 2.23.	Total revenue	46
Equation 2.24.	Average cost	46
Equation 3.1.	Cost of model	51
Equation 4.1.	Land Cost	65
Equation 4.2.	Fixed Cost	66
Equation 4.3.	Substrate Cost	66
Equation 4.4.	Total Cost	66
Equation 4.5.	Good Unit Yield	67
Equation 4.6.	Output	68
Equation 4.7.	MACM	69
Equation 4.8.	Total Revenue	69
Equation 4.9.	Molding assembly profit	73

LIST OF ABBREVIATIONS

		page
RF	Radio frequency	4
WS	Wafer Sort	6
WFT	Wafer Final Test	6
EDS	Electronic Die Sort	6
CP	Circuit Probe	6
SM	Surface Mount	6
PCB	Printed Circuit Board	6
IC	Integrated Circuit	9
N₂	Nitrogen	12
ASP	Average Selling Price	18
CAD	Computer aided design	26
KPI	Key Performance Indicators	27
OEE	Overall Equipment Efficiency	28
COO	Cost Of Ownership	28
COM	Cost Of Measurement	32
SEMI	Semiconductor Equipment and Materials International	33
FS	Initial fixed costs	35
LS	Labor cost	35
RS	Reoccurring costs	35
YS	Yield costs	36

PS	Parts cost	36
L	Entire lifetime of the equipment	37
T	Throughout rate	37
Y	Composite yield	37
U	Utilization	38
SM	Scheduled Maintenance	38
USM	Unscheduled Maintenance	38
MTBF	Mean Time Between Failure	38
MTBA	Mean Time Between Assists	38
A	Assist time	38
S	Standby time	39
Q	Qualification of the equipment	39
H	Total number of scheduled production hours per week	39
ABC	Activity-Based Costing	39
C	Test cost	42
C_{CAP}	Capital equipment cost	42
C_{CELL}	Test cell cost	42
C_{prober}	Handler Cost	42
C_{ATE0}	Base tester cost	42
C_{1Ch}	Cost per tester channel	42
N_{Ch}	Number of channel per tester	42
C_{1site}	Pre test site resources	43
S	Number of test-sites required for the testing	43

T_{Depr}	Equipment depreciation	43
P_{Util}	Utilization	43
C_{Op}	Test Operation Cost	43
R_{Op}	Fix cost rate	44
t_{Tos}	Total time in the test cell	44
k_{Conc}	Fraction of the concurring testing	44
P_{Conc}	Percentage of time can be executed	44
k_{Seq}	Fraction of sequential test	44
P_{Seq}	Percentage of the executed sequentially test time	44
k_{fail}	Fraction of the failure devices test item	44
P_{fail}	Percentage of the fail devices during testing	44
K_{retest}	Fraction for the retest devices test time	45
P_{retest}	Percentage of retesting device	45
t_{step}	Prober/handler indexing time	45
t_{test}	Total test time for one single probing	45
T_{Lot}	Production lot changeover time	45
S	Cost of each contacting sites	45
N_{Lot}	Number of devices in that lot	45
C_{PC}	Cost of probe-cards	45
N_{Spare}	Spare units	45
N_{TD}	Number of contact-sites	45
N_{LT}	Life span of the probe-card	46
C_{Pkg}	Packaging bad parts	46

E	Test Effectiveness	46
C_{TPkg}	Total packaging cost	46
C_{test}	Test Cost Model	46
ATE	Automated Test Equipment	46
C_{ate}	Cost	46
C_{opt}	ATE accessories related cost	46
C_{dib}	Circuit module related cost	46
C_o	Miscellaneous cost	46
C_{perpin}	Cost per digital pin	47
N_{pin}	Number of configured pins	47
U_{ate}	Machine utilization percentage	47
R_{dep}	Depreciation ration	47
T_{dep}	Depreciation period	47
T_o	Unit silicon test time	47
C_{dopt}	Tester accessory depreciation cost	47
M_{opt}	Fractional multiplier	47
V	Insertion volume	47
C_{dib}	Circuit module related cost	47
Chandle	Cost of handling equipment	48
C_{quality}	Quality cost	48
UPH	Unit per hour	51
D	Chip density per substrate	54
I	Indexing time	54

C	Curing time	54
ANOVA	One way Anova analyse method	58
MACM	Molding Assembly Cost Model	65
EC	Equipment cost	69
FC	Fixed cost	69
LC	Labour cost	69
LD	Land cost	69
MC	Maintenance cost	69
VC	Variable cost	69
SD	Substrate density	70
ROI	Return of Investment	109

LIST OF APPENDIXS

		Page
Appendix 1.	VARIABLES FOR CASE STUDY AND MOLDELING CALCULATION EXCEL SHEET	a
Appendix 2.	ONE WAY ANOVA AND POST HOC TEST FOR HYPOTHESIS 1: DIFFERENT SUBSTRATE VERSUS THROUGHPUT IMPROVEMENT	b
Appendix 3.	ONE WAY ANOVA AND POST HOC TEST FOR HYPOTHESIS 1: DIFFERENT SUBSTRATE VERSUS ASSEMBLY COST REDUCTION	c
Appendix 4.	ONE WAY ANOVA AND POST HOC TEST FOR HYPOTHESIS 1: DIFFERENT SUBSTRATE VERSUS ASSEMBLY YIELD	d
Appendix 5.	ONE WAY ANOVA AND POST HOC TEST FOR HYPOTHESIS 1: DIFFERENT SUBSTRATE VERSUS PROFIT	e
Appendix 6.	THE MALAYSIAN HOUSE PRICE INDEX REPORT 2011	f
Appendix 7.	F-Table	g

CHAPTER 1

INTRODUCTION

1.0. Overview

This chapter comprises two main sections: (1) an overview of the semiconductor chip industry, its manufacturing process, and the cost involved in semiconductor manufacturing; (2) the scope of research, the problem statement, and the objectives.

1.1. Research background

This section provides information on semiconductors, including overviews on semiconductor chips, semiconductor manufacturing, problem magnitude, and semiconductor assembly cost.

1.1.1. Overview of the semiconductor chip

A semiconductor is a microelectronic circuit built on a silicon wafer to perform electronic functionality on the basis of design requirements. Semiconductor chips are built with the transistor gate and have various types, such as processors, power management chips, and memory chips. Given the growing demand for electronic products with multi-functionality, small and complex designs have become the technology requirements for semiconductor chips. Process innovation is important in reducing production costs over the life cycle of a product (Hatch, 1998). Thus, process innovation strongly affects the design of semiconductor chips indirectly