MANAGING TECHNOLOGY: A CASE STUDY ON THE COST REDUCTION OF THE MOLDING ASSEMBLY PROCESS IN THE SEMICONDUCTOR INDUSTRY

KALIYAPPAN A/L P. RENGANATHAN

ASIA e UNIVERSITY
2014

MANAGING TECHNOLOGY: A CASE STUDY ON THE COST REDUCTION OF THE MOLDING ASSEMBLY PROCESS IN THE SEMICONDUCTOR INDUSTRY

KALIYAPPAN A/L P. RENGANATHAN

A Thesis Submitted to the School of Graduate Studies of
Asia e University in Fulfillment of the
Requirement for the Degree of
Master of Science (Management)
By Research

September 2014

ABSTRACT

The aim of this study is to investigate the ways in which the semiconductor industry can provide high-quality integrated circuit (IC) assembly services to satisfy customer needs and help companies introduce new products to the market in the shortest time possible. In this study, prototype ICs are assembled in production volumes that not only meet design requirements but also provide quality samples to customers. To increase the cost effectiveness of the component assembly process, the cost of the existing process was determined and a mathematical formula developed to predict the outcome of changes applied in the process (Ragona, 2002).

Over the years, the performance of the semiconductor chip has been significantly improved to meet the current market demand for electronics devices, such as smartphones, personal computers, and car navigation systems. The transistor is the main component of the semiconductor chip. Therefore, the performance of the transistor is important because it significantly influences the density of the transistor per chip (Gordon, 1965).

An increase in the capacity of the transistor per chip increases the manufacturing cost. For this case, various methods and strategies have been implemented to ensure that chip suppliers remain competitive in the market.

This research used the high density substrate approach to analyzed the cost of assembly and molding profit through the models which were developed from economics theory of the firm models namely the average cost model and the profit model by integrated in the molding technology aspect particularly the high density substrate. The new models which were developed by the author are the Molding Assembly Cost Model (MACM) and the Molding Assembly Profit Model (MAP).

4 hypotheses were developed to compare the high density substrate versus the low density substrate. The hypotheses for this comparison are the throughput, the yield, the assembly cost and finally the profit.

The author concluded that the high-density substrate approach is sufficient to guarantee of the assembly cost reduction hence improvement of the profit with the condition that the assembly yield must remain stable.

APPROVAL PAGE

I certify that I supervised/read this study. In my opinion, this study conforms to the acceptable standards of scholarly presentation and is fully adequate, in quality and in scope, as a thesis for the fulfillment of the requirements for the degree of Master of Science (Management) by Research.

.....

Dr. Ian Mackechnie
Supervisor

.....

Dr. J Janet Lourds Rani
External Examiner

.....

Dr. Oo Yu Hook
Internal Examiner

.....

Prof. Dato' Dr Sayed Mushtaq Hussain
Chairman, Examination Committee

This thesis was submitted to the School of Management of Asia e University and was accepted in fulfillment of the requirements for the degree of Master of Science (Management) by Research.

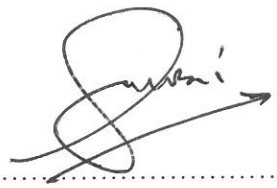
.....

Prof. Dr. Juhari Hj Ali
Dean, School of Management

Declaration

I hereby declare that this thesis is my own work and that all contributions from other persons or sources have been properly and duly cited. I further declare that the materials in this thesis have not been submitted, either in whole or in part, to any other degree in this or any other university. I understand and acknowledge that any breaches in this declaration will constitute academic misconduct, which may lead to my expulsion from the program and/or exclusion from the degree.

NAME: KALIYAPPAN A/L P. RENGANATHAN



.....

SIGNATURE OF THE CANDIDATE: DATE: 2 SEPTEMBER 2014

ACKNOWLEDGEMENT

In humility, I thank GOD for the completion of this thesis. The research work presented here was conducted in fulfilment of the requirements of Asia e University for the Master of Science (MANAGEMENT) By Research degree in the School of Management, from September 2010 to September 2014.

I dedicate this work to my beloved parents -the late Mr. P. Renganathan and Mrs. M. Anjalai – whose unfailing support provided the moral encouragement and motivation throughout the course of my research. I record my heartfelt gratitude and dedicate this thesis in memory of my father who passed away on 13 May, 2014.

I am thankful to my supervisor, Dr Ian Mackechnie, for his thoughtful supervision, steady support and guidance throughout my research. I also thank the School of Management for its support during my candidature.

I am grateful to the Company and the Engineering Manager for permitting me to conduct this research in their premises. The on-site research would not have been completed without their support.

And I am thankful for the administrative, encouraging and student-friendly support given by Professor Dr Oo Yu Hock, the SOM MSc Program Coordinator and SGS Academic Advisor of PhD (BA) candidates in AeU in the final stages of completing my study.

Lastly, I extend my heartfelf gratitude to my beloved wife – Pushpalatha, and my children, sisters, brothers, uncles, aunts, friends and other close family members, particularly Mr. Rajendran and Mrs. Mankairasi who provided me with love, inspiration and confidence. THANK YOU for always being there for me and making this academic pursuit worthwhile.

Kaliyappan s/o P. Renganathan
Monday, 25 August 2014 [viva voce]

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

CHAPTER 2

LITERATURE REVIEW

CHAPTER 3

RESEARCH METHODOLOGY

CHAPTER 4

DEVELOPMENT OF ASSEMBLY COST MODEL AND MOLDING PROFIT MODEL

CHAPTER 7

Conclusion and recommendation

LIST OF TABLES

LIST OF FIGURES

LIST OF EQUATION

LIST OF ABBREVIATIONS

		page
RF	Radio frequency	4
WS	Wafer Sort	6
WFT	Wafer Final Test	6
EDS	Electronic Die Sort	6
CP	Circuit Probe	6
SM	Surface Mount	6
PCB	Printed Circuit Board	6
IC	Integrated Circuit	9
N_2	Nitrogen	12
ASP	Average Selling Price	18
CAD	Computer aided design	26
KPI	Key Performance Indicators	27
OEE	Overall Equipment Efficiency	28
COO	Cost Of Ownership	28
COM	Cost Of Measurement	32
SEMI	Semiconductor Equipment and Materials International	33
F$	Initial fixed costs	35
L$	Labor cost	35
R$	Reoccurring costs	35
Y$	Yield costs	36

P$	Parts cost	36
L	Entire lifetime of the equipment	37
T	Throughout rate	37
Y	Composite yield	37
U	Utilization	38
SM	Scheduled Maintenance	38
USM	Unscheduled Maintenance	38
MTBF	Mean Time Between Failure	38
MTBA	Mean Time Between Assists	38
A	Assist time	38
S	Standby time	39
Q	Qualification of the equipment	39
H	Total number of scheduled production hours per week	39
ABC	Activity-Based Costing	39
C	Test cost	42
C_{CAP}	Capital equipment cost	42
C_{CELL}	Test cell cost	42
C_{prober}	Handler Cost	42
C_{ATE0}	Base tester cost	42
C_{ICh}	Cost per tester channel	42
N_{Ch}	Number of channel per tester	42
C_{1site}	Pre test site resources	43
S	Number of test-sites required for the testing	43

E	Test Effectiveness	46
C_{TPkg}	Total packaging cost	46
C_{test}	Test Cost Model	46
ATE	Automated Test Equipment	46
C_{ate}	Cost	46
C_{opt}	ATE accessories related cost	46
C_{dib}	Circuit module related cost	46
C_o	Miscellaneous cost	46
C_{perpin}	Cost per digital pin	47
N_{pin}	Number of configured pins	47
U_{ate}	Machine utilization percentage	47
R_{dep}	Depreciation ration	47
T_{dep}	Depreciation period	47
T_o	Unit silicon test time	47
C_{dopt}	Tester accessory depreciation cost	47
M_{opt}	Fractional multiplier	47
V	Insertion volume	47
C_{dib}	Circuit module related cost	47
Chandle	Cost of handling equipment	48
Cquality	Quality cost	48
UPH	Unit per hour	51
D	Chip density per substrate	54
I	Indexing time	54

C	Curing time	54
ANOVA	One way Anova analyse method	58
MACM	Molding Assembly Cost Model	65
EC	Equipment cost	69
FC	Fixed cost	69
LC	Labour cost	69
LD	Land cost	69
MC	Maintenance cost	69
VC	Variable cost	69
SD	Substrate density	70
ROI	Return of Investment	109

LIST OF APPENDIXS

CHAPTER 1

INTRODUCTION

1.0. Overview

This chapter comprises two main sections: (1) an overview of the semiconductor chip industry, its manufacturing process, and the cost involved in semiconductor manufacturing; (2) the scope of research, the problem statement, and the objectives.

1.1. Research background

This section provides information on semiconductors, including overviews on semiconductor chips, semiconductor manufacturing, problem magnitude, and semiconductor assembly cost.

1.1.1. Overview of the semiconductor chip

A semiconductor is a microelectronic circuit built on a silicon wafer to perform electronic functionality on the basis of design requirements. Semiconductor chips are built with the transistor gate and have various types, such as processors, power management chips, and memory chips. Given the growing demand for electronic products with multi-functionality, small and complex designs have become the technology requirements for semiconductor chips. Process innovation is important in reducing production costs over the life cycle of a product (Hatch, 1998). Thus, process innovation strongly affects the design of semiconductor chips indirectly