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A Cost Of Test Case Study For Wafer-Ring Multi-Sites Test Handler In Semiconductor's Industry Through Theory Of The Firm

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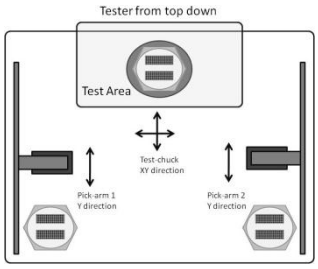
Graphical abstract



Abstract

In this research, the author conducted the cost of test study for the wafer-ring test handler in semiconductor's industry with theory of the firm model. A cost of test model have been developed through the theory of the firm average cost theory by integrated the technology aspect into it so that the cost study can be conduct. The aim of this research is to find out the effectiveness of the wafer-ring test handler in order to reduce the cost of testing. Wafer-ring test handler is the invented technology which have been developed for Wafer-level Packaging (WLP), Chip-Scale Package (CSP) and QFN testing whereby those semiconductor's devices are the next generation device for the purpose of to simplified the manufacturing process ultimately to reduce the manufacturing cost in total. The manufacturing cost in the semiconductor's industry included of assembly cost and testing cost hence the said devices managed to simplified the assembly process and reduce the cost of assembly but if the testing-cost is not reduce in parallel, it will affected the profit margin. This study is important as a guideline for the semiconductor industry in terms of cost control to maintain the profit margin due to the depreciation of the average selling price (ASP) for past 20 years.

Keywords: Cost of Test; Testing economic model; Multi-sites testing; wafer-ring test handler

1.0 INTRODUCTION

Electronic devices, such as personal computers and cell phones, continue to reduce their selling price as a marketing strategy to maintain their position in the market and to stay competitive. For example, the Apple Macintosh with a speed of 8 MHz was launched in 1984 and sold for $1,995 USD to $2,495 USD (http://en.wikipedia.org/wiki/Macintosh; cited: 11 April 2012). The latest generation of the Macintosh family, the I-Mac 2.5 GHz to 3.1 GHz, which is approximately a thousand times faster than the original Macintosh, only sells at a price range of between $1,199 USD to $1,699 USD (http://store.apple.com/us/browse/home/shop_mac/family/imac/select; cited: 11 April 2012).

Although the speed of the Macintosh has increased 1000 times and more advanced features have been added to it, its price has decreased by approximately 47%. This example shows that products with high-performance semiconductor chips are not being sold at the price that people expected 20 years ago.

Companies are doing an excellent job of reducing fabrication cost by 25% to 30% (Goodall, 2002) over the past 50 years. Figure 1 shows that fabrication cost was predicted to decrease from 1 US cent per transistor in 1982 to 0.0001 US cent per transistor in 2012. However, the cost of testing has increased. In 2012, the cost of testing equaled the cost of fabrication (Bao, 2003).

Nowadays, fabrication cost is no longer the deciding factor for profit margin in the manufacture of semiconductor chips. Therefore, to reduce fabrication cost and the subsequent increase in testing cost, semiconductor manufacturers must continue to improve their "testing technology." Doing so will also allow them to stay competitive in the market. If the cost of testing is not reduced, the procedure will have a negative effect on the overall manufacturing cost of semiconductor chips in the future.

With the increasing demand for high-complexity consumer Electronic products, the design of New Semiconductor chips needs to provide the required flexibility and speed. This trend shows that the functionality built into a single Semiconductor chip has continuously improved compared to the functionality 20 years ago. In contrast, Testing Costs in Semiconductor industries today can reach a substantial percent of the total Manufacturing Cost, thus affecting the Profit Margin.

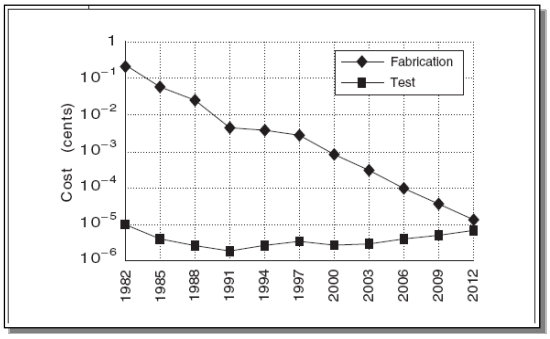


Figure 1 Cost of testing a transistor approximates the cost of fabricating it (bao g., 2003)

Numerous Approaches have been introduced to lessen Testing Costs; one of them is the Multi-site Testing. A Case Study was conducted to determine the effectiveness of Multi-site Testing in reducing Testing Costs. To achieve the research goal, a Multi-site test Cost Model was developed based on the economic theory of the firm-Average Cost theory, by integrating important elements into the Model such as the technology Multi-site efficiency etc. Through the developed Model, this research managed to measure the capabilities of the Multi-site testing for the Cost of Test Deduction.

The case Studies were conducted on Wafer-ring Test-equipment. Five Multi-site configurations were configured on the Test-equipment setup for comparison. Testing time, indexing time, and Testing yield data were collected for the purpose of establishing the Testing Cost. The Hypothesis which was designed to analyze the performance of the Test-equipment setup is Multi-site versus Testing Cost. The hypothesis was analyzed using one-way ANOVA and Post-hoc test.

This research found that increasing the number of test sites is not sufficient to guarantee reduced Testing Cost while maintaining Profit Margin because once the number of test sites increase in parallel, the Testing time will increase as well. In this case, this research proposed that future work be conducted on the Multi-site Testing Approach together with other Testing Approaches that can reduce Testing time, such as concurrent Testing.

■2.0 THE WAFER-RING HANDLER

The concept of the wafer-ring testing handling is similar to that of the lead frame strip testing. However, this handling method attaches the lead frame on top of the wafer ring. A photograph of the wafer-ring is shown in Figure 2. This testing method is used on lead-less packagers such as wafer-level packaging, ball-guided assembly, chip scale packaging, and so on.

Similar to lead frame strip-testing handling, the semiconductor chip is tested without singulating the chip from the leadframe. As shown in Figure 3 below, the process flow is basically similar to that of leadframe strip- testing handling, the only difference being the wafer ring, which is attached to the two leadframes, is transferred to the Test Area by pick-arm 1 and attached to the test chuck. The test chuck then transfers the wafer ring to the Test Area and, similar to the lead-frame testing handling, the wafer is punched to connect to the test socket/contactor. The test chuck moves in X and Y directions to test the entire chip on the wafer ring. The completely tested wafer ring is transferred to the output area by pick-arm 2. A photograph of the wafer ring test chuck is shown in Figure 4 below.

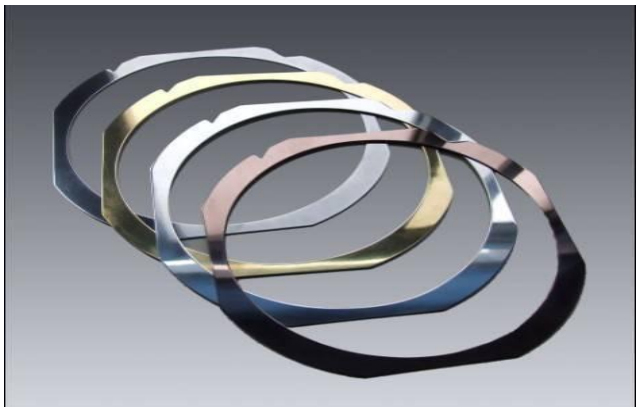


Figure 2 Example of Wafer Rings

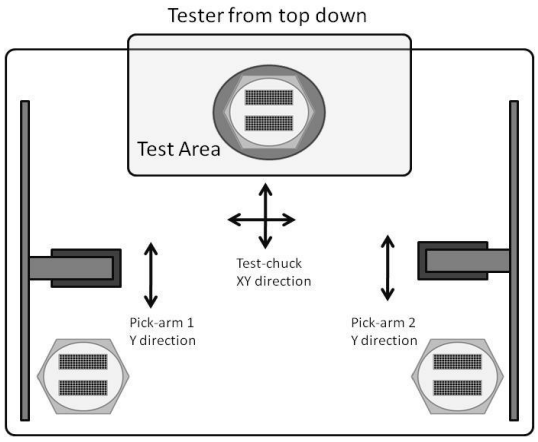


Figure 3 The process flow of the wafer-ring testing-handling test equipment

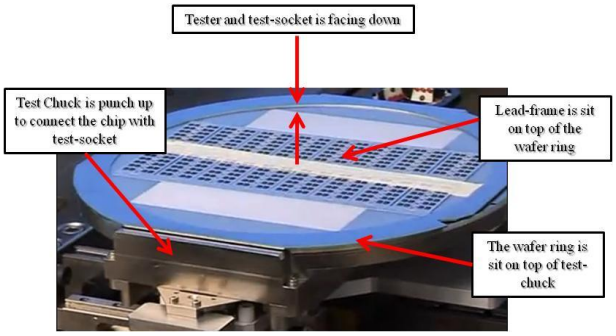


Figure 4 The test chuck of the wafer-ring testing handling

■3.0 COST MODEL DEVELOPMENT

The cost-of-test model in this research was developed based on average cost theory, as shown in Equation 1. Average cost theory involves two elements: total cost and production output.

$$\text{Average Total Cost (ATC)} = \frac{\text{Total Cost (TC)}}{\text{Output (Q)}} \quad (1)$$

3.1 Total Cost

According to the average total cost theory, the total cost included of fixed cost and the variable cost. For the multi-sites testing aspect, the variables which affected the total cost are shown in table 1 as below.

Table 1 Multi-sites testing variable for total cost.

Total Cost	
Fixed Cost	**Variable Cost**
Depreciation Cost i. Tester Cost ii. Test Handler Cost	**Bad Parts Cost**
Direct Labor Cost i. Operator Salary ii. Technician Salary	
Overhead Cost i. Management Cost - Manager's salary - Supervisor's salary - Engineer's salary ii. Facility cost - Electricity cost, compress air cost etc iii. Floor space cost iv. Maintenance cost - Wear and tear parts - Consumable parts etc v. Test accessories cost - Test socket/contactor - Test Load board	

3.1.1 Fixed Cost

Whereby the fixed cost included of equipment depreciation cost (Dep) which contain of the tester cost and the test handler cost. Equation 2 was developed to calculate the equipment depreciation cost which span over five years from it purchase value to zero-cost.

$$\text{Dep} = \left(\frac{\text{Tester Cost} + \text{Handler Cost}}{5}\right) \div 12. \quad (2)$$

The second variable which affected the fixed cost is the direct labor cost (DL). The direct labor (DL) cost is the monthly salary of employees who directly contributes to the production output, such as operators and technicians. Direct labor cost is expressed in Equation 3:

$$\text{Direct Labor Cost per month} = \left(\text{Operator salary per month} \times 3\right) + \left(\text{Technician salary per month} \times 1.5\right) \quad (3)$$

For the operator variable, each test-equipment setup requires one operator, and thus, three operators are needed each day to cover three production shifts. For one shift, only one operator is required. To standardize the equation for ease of understanding, three shifts are used in this study.

For the technician variable, one technician can support two test-equipment setups. Therefore, only a half the cost is needed per test-equipment setup. To cover three production shifts, only 1.5 technicians are needed.

Operator and technician wages are based on a report published by JobStreet.com. (cited: 11 April 2012). In this study, the average wage is used as a reference for the aforementioned positions.

In addition, the Overhead (OH) cost is the cost incurred during production aside from equipment depreciation and direct labor costs. Overhead cost includes the following.

- Management Cost includes the monthly wages of the manager, supervisor, and engineer, which are considered as indirect labor costs. Wages data are based on a JobStreet.com report (cited: 11 April 2012). Equation 4 shows management cost calculation:

$$\text{Management cost} = \text{Manager's Salary} + \text{Supervisor's Salary} + \text{Engineer's Salary} \quad (4)$$

- Facility Cost is the monthly utility cost of electricity, compressed air, and so on.
- Floor-Space Cost (FPS) is the cost of the area occupied by the test-equipment setup. Equation 5 shows the calculation of floor space cost:

$$\text{FPS} = \left(\frac{\text{(Selling Price)}}{3000}\right) \text{X} \begin{array}{c}\text{Test Equipment}\\ \text{floor space area}\\ \text{(Sq-Ft)}\end{array} \quad (5)$$

In this study, the calculation of floor-space cost is based on the Malaysian Government Valuation and Property Service Department Report 2011. The 2011 "Detached House Pricing" is adopted as a reference for calculating price per sq. ft. Test equipment setup floor space costs are then calculated as the X number of area sq. ft. needed multiplied by the per sq. ft. pricing, as shown in Equation 5.

- Maintenance Cost is the cost spent in one month to maintain the test equipment, such as wear-and-tear part cost, consumable part cost, and so on. The study estimates maintenance cost at 5% per year of the test equipment cost.
- Cost-of-Test Accessories includes the test contactor and load board, which are described as follows:
- Load Board/Probe Card is the electronic printed circuit board used for interfacing between the tester and the test handler.
- Test Contact Socket is the mechanism used to connect the semiconductor device to the load board.

3.1.2 Variable Cost

Another factor identified as part of the total cost calculation that has an effect on the test yield is the variable cost. From the research point of view, the variable cost is categorized as a changeable cost because it is not fixed, and it will change when the testing yield is modified.

The variable cost that needs to be included is the bad-part cost based on the test cost model developed by Rivoire (2003). The bad-part cost is imperative in this research, particularly when dealing with multi-site configurations, because the developed model will be validated using this configuration. When changes are implemented during testing, they may affect the consistency of the testing yield, which depends on multi-site repeatability efficiency.

To include the bad-part cost into the total cost equation, an equation has to be derived to calculate the cost of bad parts. The first step in deriving the bad-part cost equation is to imply the appropriate equation that can calculate the quantity of bad parts.

Equation 6 is derived for this purpose.

$$\text{Number of bad part} = \text{Total Input X } \left[100\% - (\text{Testing Yield})\right] \quad (6)$$

Based on Equation 6, total incoming chip quantity is multiplied by the bad part yield, which can be obtained by deducting the testing yield from 100%. The testing yield is the tested good part percentage that can be obtained from Equation 7:

$$\text{Testing yield \%} = \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (7)$$

Finally, to calculate the cost of the tested bad parts, the ASP of a particular type of semiconductor chip is multiplied with the number of bad parts obtained from Equation 6. Therefore, Equation 8 is derived to determine the total cost of tested parts.

$$C_{Pkg} = \text{ASP} \left[\text{Total Input X} \left(\text{ Bad part \% } \right) \right] \quad (8)$$

where:
- CPKg is the cost of bad parts;
- ASP is the average selling price;
- Total Input is the total input of semiconductor chips; and
- Bad Part % is the tested bad chips obtained by deducting the testing yield from 100%.

All costs have been discussed thoroughly to facilitate total cost calculation. Therefore, by putting together all the equations, Equation 9 is derived to demonstrate how the total cost has been integrated:

$$\text{Total Cost} = \text{Dep} + \text{DL} + \text{OH} + C_{Pkg.} \quad (9)$$

Another element incorporated in average cost theory for the developed model is production output. A detailed discussion of this element is provided in the following subsection:-

3.2 Production Output

Production output consists of three fundamentals: testing output (throughput), testing yield, and the equipment utilization percentage. Detailed explanations for these fundamentals are as follows.

$$UPH_{good} = \frac{3600 \text{ X N}}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1))} \text{ X} \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (10)$$

Equation 10 was developed to calculate the production throughput whereby the throughput obtained is the tested good product by take into account the testing yield whereby the testing yield mean that the percentage of tested good. The equation of testing yield % is shown in equation 7 in this paper.

The equation 10 was integrated with the Multi-sites efficiency (MSE) as well so that the comparison between the multi-sites versus the multi-sites efficiency (MSE) can be obtained, but in this paper will not analyze of this hypothesis and will reserve for next paper publication.

To integrate the MSE into the equation, the throughput equation from Evans (1999) as shown in equation 11 need to further enhance. Following discuss step by step on how the MSE was integrated into the throughput equation.

$$UPH_{insertions} = \frac{3600 \text{ x } n}{t_{ms} + i_{ms}} \quad (11)$$

where:
- tms is the multi-site test time, that is, the time spent to complete the testing of a semiconductor chip.
- ims is the multi-site indexing time, that is, the semiconductor chip exchange time within the tested chip replaced with a new untested chip.
- n is the number of test sites, that is, the number of semiconductor chips tested in a single contact.

To achieve the integration with the MSE, the throughput equation developed by Evans (1999), shown as Equation 11, is enhanced by integrating the MSE model developed by Kelly (2008). The MSE proposed by Kelly is presented as Equation 12:

$$MSE = \left(1 - \frac{\Delta t}{\Delta N(t_1)} \right) .100\% \quad (12)$$

where:
- Δt is the change in testing time between single-site and multi-site testing; and
- ΔN is the number of different test sites between single-site and multi-site testing.

Equation 12 is further derived, as shown in Equation 13.

$$MSE = \left(1 - \frac{(t_{MS} - t_1)}{(N\text{-}1)(t_1)} \right) .100\% \quad (13)$$

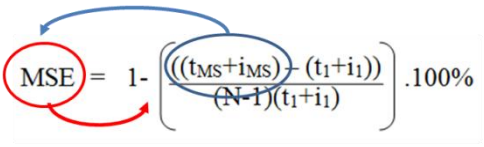
where:
- t_{MS} is the multi-site test time, and t1 is the single-site test time; and
- N is the number of test sites for multi-site testing.

The test handler affects testing throughput. Therefore, the test handler indexing time has to be included as part of the MSE equation. In doing so, Equation 14 is derived by including the indexing time (i), as follows:

$$MSE = 1 - \left(\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N\text{-}1)(t_1+i_1)} \right) .100\% \quad (14)$$

For the integration of the equations to work, one must have prior understanding of the relationship between the throughputs and MSE. To determine the relationship between MSE and multi-site, the variables of MSE, which is related to the throughput, need to be understood. Equation 11 and Equation 14 show that the multi-site test time (t_{ms}) and multi-site indexing time (i_{ms}) are common variables in both equations.

In Equation 14, t_{MS} and i_{MS} represent multi-site test time and indexing time. Therefore, to clearly derive the relationship between t_{ms} and i_{ms} in relation to MSE, the integration process shown in Figure 5 is carried out.



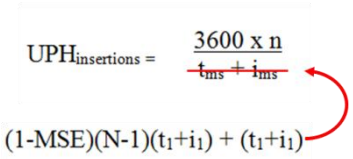
Source: Author's own research

Figure 5 Deriving the Relationship between t_{ms} and i_{ms} with MSE

As Figure 5 illustrates, t_{ms} and i_{ms} move to the left side of the equation, whereas MSE moves to the right side. The final computation for the equation of t_{ms} and i_{ms} in relation to MSE is derived and shown in Equation 15.

$$(t_{MS} + i_{MS}) = (1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1). \quad (15)$$

Finally, Equation 15 is integrated into Equation 11 to obtain the computation for testing throughput, which includes MSE as part of the calculation. Figure 6 below shows the computation of the integration, and the complete integration is illustrated in Equation 16:



Source: Author's own research

Figure 6 The computation of the integration of equation 15 into equation 11

$$UPH_{insertions} = \frac{3600 \text{ X } N}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1)),} \quad (16)$$

where:

$UPH_{insertions}$ are represented by the testing output in one hour.

A. Equipment Utilization (U)

Equipment utilization percentage refers to the percentage by which the test equipment is used in producing output. When the test equipment is 100% utilized, then no cost is lost. The aforementioned cost refers to the total cost, as indicated in Equation 9. When equipment utilization achieves a higher percentage, the cost becomes cheaper. By contrast, when utilization percentage begins to decrease, then the cost increases (Horgan, 2004).

Given that equipment utilization percentage affects the total cost, then the former must be included in Equation 9. Therefore, the total cost equation, which involves equipment utilization percentage, is depicted in Equation 17.

$$\text{Total Cost per month} = \frac{(\text{Dep} + \text{DL} + \text{OH} + C_{Pkg})}{U} \quad (17)$$

The total cost obtained from Equation 17 is the monthly testing expenditure. However, the testing throughput is calculated based on the hourly production output. Therefore, to obtain the total cost per hour, Equation 17 has to be further derived, as shown in Equation 18.

$$\text{Total Cost per hour} = \frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + C_{Pkg}}{729.6}\right)}{U} \quad (18)$$

Where the total cost is divided by 729.6 to obtain the hourly cost; and 729.6 is the total number of production hours in one month.

After all the equations and variables for average cost theory are defined, the next step is to integrate all the equations into average cost theory to derive the cost of the model. The integration is illustrated in Figure 7:

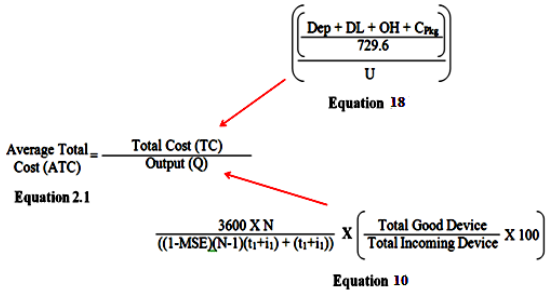


Figure 7 The integration of equations 18 and 10 into equation 1.

As shown in Figure 7, the average cost in Equation 1 is integrated with Equation 18, which is the total cost in one hour, and Equation 10, which is the total number of good chips tested in one hour.

The final cost of test model is then integrated, as shown in Equation 19:

$$CPU_{GOOD} = \frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{U}\right)}{\left(\frac{3600 \text{ X } N}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1))}\right) \text{ X } \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100\right)} \quad (19)$$

The following section discuss of the wafer-ring Test Equipment's Multi-sites configuration for this study.

■4.0 WAFER-RING TEST-EQUIPMENT'S MULTI-SITES CONFIGURATION

The wafer-ring test equipment can support the configuration of X32-sites. Wafer-ring testing attaches two lead frames on a wafer ring. Test site configurations are on the lead-frame layout for the setting from a single-site to X32-sites.The top-view illustration of the lead frame is shown in Figure 8 below:-

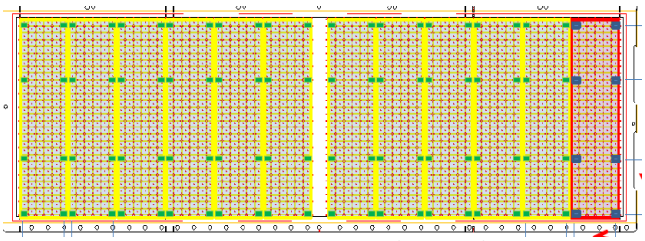


Figure 8 Top view illustration of the lead frame

For single-site testing, the wafer-ring test equipment is configured to allowcontact with one chip (represented by a bluebox) on the leadframe per touchdown, and is indexed to the next chip in the direction of the red arrow,as shown in Figure 9 below. The test equipment completes testing the entire chip in the first row before moving on to the second row to perform the same sequence.

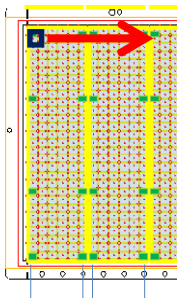


Figure 9 Single-site testing sequence for wafer ring testing

The sequence for quad-site testing is similar to that for single-site testing. However, the test equipment comes in contact with four chips per touchdown, as shown in Figure 10 below. After testing the first four chips, the equipment will then index toward the direction of the red arrow. After testing the first row, the equipment will continue testing the second row by following the same sequence.

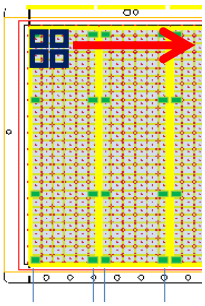


Figure 10 Quad-sites testing sequence for wafer ring testing

Octal-site, X16-site, and X32-site testing have a sequence similar to that of single-site and quad-site testing. However, for octal-site testing, the test equipment comes in contact with eight chips per touchdown, followed by 16 chips per touchdown for X16-site testing, and 32 chips per touchdown for X32-site testing, as shown in Figures 11, 12, and 13, respectively.

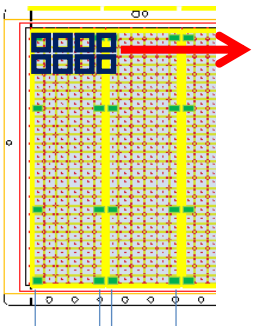


Figure 11 Octal-sites testing sequence for wafer-ring testing

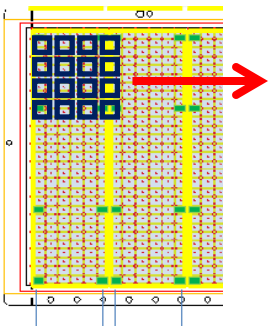


Figure 12 X16-sites testing sequence for wafer-ring testing

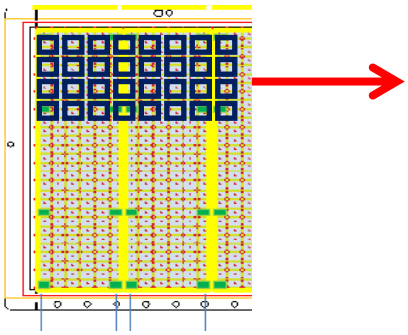


Figure 13 X32-sites testing sequence for wafer-ring testing

After defining the test-site configuration for both types of test equipment, the next step is to decide the indexing time and test-time data collection area for the test equipment.

This study only considers the pure indexing time and rejects any indexing time that causes a slow down because of external factors such as wafer-ring transferring process, loading-and-unloading process, equipment jamming, and so on. Production data are only accepted if no external factors such as handler downtime, tester downtime, and others are found.

This study only focuses on the area marked by the red circle in Figure 14 below:-

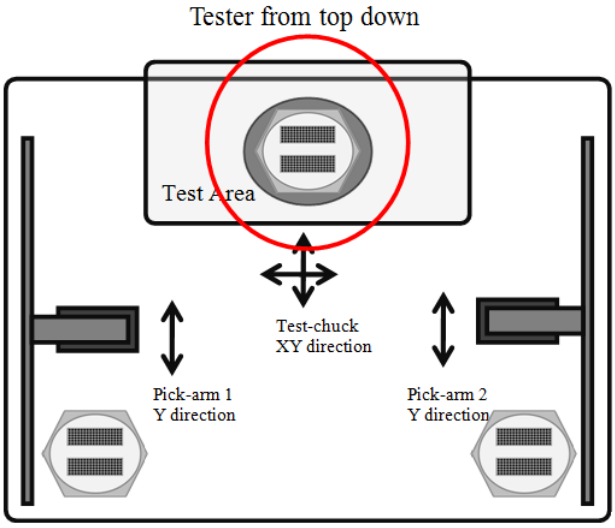


Figure 14 Focus of the research area

The indexing time is considered valid when the wafer-ring is within the red circle. Once the wafer-ring gets outside the red circle for the wafer-ring exchange, the delay time for the exchange is no longer considered because it is an external factor.

Otherwise, if the wafer-ring test equipment stops because of any external factors such as jamming, equipment downtime, time of handler and tester, new production lot loading, unloading time, and others, then the indexing time is not considered valid.

The test-time is considered valid if no external factors, such as tester downtime and chip contacting problems, cause a high rejection rate of the chip being tested.

To collect sufficient data for the cost-of-test, data size of the 30 sets of production lots for each test site configuration (single-site, quad-sites, octal-sites, X16-sites, and X32-sites) has to be collected (the data type to be collected is discussed in the following section). Each set of data contains 100 trial runs of the test-equipment setup, and thus, the 30 sets of data contain 3,000 test equipment trial runs. Five test-site configurations are employed in the case study; therefore, 30 sets are used for each test-site setup. The five types of test-site configurations contain 150 sets of data, including 15,000 trial runs on test equipment for the case study.

5.0 RESULTS AND DISCUSSION

The fixed costs for this case study are tabulated in table 2:

Table 2 The fixed costs.

Variables	Cost (RM)
Depreciation Cost/month	55417
Direct Labor Cost/month	7843
Overhead Cost/month	37613

The cost of bad parts is calculated using Equation 8, which involves an ASP of RM4.95 for the logic device. The cost of bad parts is affected by the testing yield. The summary of the cost of bad parts is shown in Table 2.

Table 3 The cost of bad parts.

Test-site configurations	Cost of bad parts
Single-site	RM50.53
Quad-sites	RM68.69
Octal-sites	RM74.48
X16-sites	RM99.25
X32-sites	RM84.90

The testing Throughput results for Wafer-ring Test-Equipment are summarized in Table 4 below:-

Table 4 Testing throughput for wafer ring test-equipment.

Test-site configurations	Throughput
Single-site	3365
Quad-sites	4626
Octal-sites	4702
X16-sites	4736
X32-sites	4390

Testing yield is one of the factors affecting the cost-of-test. Testing yield percentage data collected from the wafer-ring test-equipment setup is shown in Table 5 below:-

Table 5 Average testing yield %.

Test-site configurations	Average Testing Yield %
Single-site	99.70%
Quad-sites	99.70%
Octal-sites	99.68%
X16-sites	99.58%
X32-sites	99.61%

After obtained all the required variables, the cost of good units is calculated using Equation 19 whereby the summary is tabulated in table 6 as below:-

Table 6 Cost of good unit.

Test-site configurations	Cost of Good Unit (RM)
Single-site	RM0.0412
Quad-sites	RM0.0304
Octal-sites	RM0.0303
X16-sites	RM0.0311
X32-sites	RM0.0355

Following section discuss the data analysis through the one way ANOVA and Post Hoc Test.

An alpha level of 0.05 is used for the analysis. As previously discussed, five independent levels of configurations (a) are selected, namely, single-site, quad-sites, octal-sites, X16-sites, and X32-sites. Each independent level contains 30 data sets (n). In this case, the following data are determined:-

a = 5 independent levels,
n = 30 sets of data,
N = 150.

Therefore, the degrees of freedom are calculated as

dfBetween= 5 -1 = 4,
dfWithin = 150 – 5 = 145,
dfTotal= 150 – 1 = 149.

From the degrees of freedom between and within, which is (4,145), refer to the F-Table, with the critical value obtained as 2.3719. As indicated in the previous chapter, if the F-value is smaller than the critical value, then the null hypothesis is accepted; otherwise, the null hypothesis is rejected.

Refer to Table 5 for the summary of the cost of good unit for Wafer-ring test equipment for all test-site configurations. An analysis of the hypothesis is provided in the following sections:-

The hypothesis for the cost of good-unit analysis is as follows.

H0: Improvement of the test site has no effect on cost of good unit.
H1: Improvement of the test site has an effect on cost of good unit.

The dependence level for cost of good unit is rated on a scale of 1 to 10 and it is shown in Table 7 below:-

Table 7 Scale of cost of good-unit dependence level.

Cost of Good Unit	Scale
0.0435	10
0.0420	
0.0419	9
0.0404	
0.0403	8
0.0388	
0.0387	7
0.0373	
0.0372	6
0.0357	
0.0356	5
0.0341	
0.0340	4
0.0326	
0.0325	3
0.0310	
0.0309	2
0.0294	
0.0293	1
0.0279	

The dependence level for the cost of good unit is scaled at level one, as the cheapest cost of good unit from RM0.0279 per chip, to level ten, as the highest cost of good unit at RM0.0435 per chip. Level increment resolution is RM0.0016, as shown in Table 7.

Table 8 ANOVA results for cost of good unit.

ANOVA Table

	SS	df	MS	F
Between	1058.173	4	264.543	872.452
Within	43.96667	145	0.30322	
Total	1102.14	149	7.397	

The one-way ANOVA results for the wafer-ring test equipment are shown in Table 8 with the F-value at 872.45, which is higher than the critical value of 2.3719. Thus, the analysis suggests a rejection of the null hypothesis and acceptance of the alternative hypothesis, that is, improvement of test sites has an effect on the cost of good unit for the wafer-ring test equipment. Thus, a post hoc test is conducted to analyze the difference among test sites.

Table 9 Post hoc test analysis results for cost of good unit.

Post Hoc Test

Independence Level	F-value	Analysis Result
Single vs. Quad	583.133	Different - Reject the null hypothesis
Single vs. Octal	617.597	Different - Reject the null hypothesis
Single vs. X16	490.859	Different - Reject the null hypothesis
Single vs. x32	201.189	Different - Reject the null hypothesis
Quad vs. Octal	0.495	No Difference - Accept the null hypothesis
Quad vs. X16	3.971	Different - Reject the null hypothesis
Quad vs. X32	99.282	Different - Reject the null hypothesis
Octal vs. X16	7.269	Different - Reject the null hypothesis
Octal vs. X32	113.793	Different - Reject the null hypothesis
X16 vs. X32	63.541	Different - Reject the null hypothesis

The post hoc test analysis results for the wafer-ring test equipment are shown in Table 5.47. Only the quad-sites and the octal-sites do not have significant cost of good-unit improvements. Analysis of the results shows that the octal-sites exhibit higher improvements compared with the single-site testing. Thus, the octal-site configuration produces the chip at the cheapest cost among the test-site configurations, followed by the quad-site configuration. The X16-sites produce the second highest cost of goods unit, and the X32-sites configuration incurs the most expensive testing cost among all test-site configurations.

5.0 CONCLUSION

The total cost and production output affect testing cost, as validated by this study. Production output is affected by MSE, and a higher MSE results in better production output.

The MSE is determined based on the indexing time, test time, and number of test sites. Production output increases when the indexing and test times are decreased, and the increment in the number of test sites contributes to the improvement of the production output. However, if the increment in the number of test sites affects the indexing time and test time is increased at the same time, then the MSE decreases. A lower MSE results in lower production output. Therefore, combining the three variables, namely, indexing time, test time, and number of test sites, determines the MSE, which directly contributes to the production output.

The validation process proves that increments in the number of test sites do not necessarily reduce the testing cost. This study shows that increasing the number of test sites does not guarantee improved throughput and testing cost. The main reasons for this situation are presented in Figure 15.

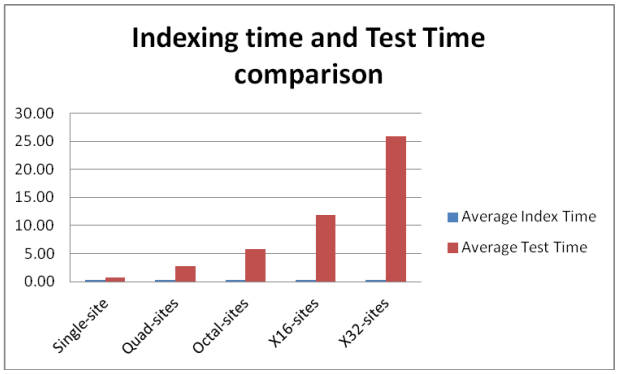


Figure 15 Comparison of the indexing time and test time for the wafer-ring test equipment.

Testing throughput, which is the main contributor to the testing cost, is affected by the indexing and test times. Figure 15 depicts that the test time for the test equipment significantly increases once it reaches a higher test site configuration although the indexing time for the test equipment setup increases steadily. Therefore, the test time induces decreases in testing speed and testing throughput, which increases testing cost and decreases profit margin.

This study concludes that simply increasing the number of test sites is insufficient to improve testing throughput. Instead, the test time must also be reduced. The test time can be reduced through different means, including reduced pin-count testing and concurrent testing.

Future Work.

A number of future research directions based on the current study that can contribute to the development of low-cost testing are briefly outlined as follows:-

i. Conducting a multi-site case study, combined with testing-time improvement methods such as the concurrent testing approach and reducing pin-count testing, can be used to study the effectiveness of the combination and their contribution to the reduction f-testing cost. Future research can be directed at collecting further data and constructing a multi-site table that can provide information on how many testing times are allowed for a test-site configuration setup to improve the profit margin.

ii. The profit-margin and cost-of-test models can be improved further by integrating the models with an ASP-prediction function for the next 10 years. This will enable the subsequent developed model to predict the cost of testing per chip for the aforementioned period. Test-equipment developers can benefit from such a new model and can manufacture test equipment capable of supporting future requirements of the industry.

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